Notice of Allowability	Application No.	Applicant(s)	
	10/827,432	XIANG, QI	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Prelim. Amdt. 4/20/04*.

2. ☒ The allowed claim(s) is/are *1-11*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 4/20/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-11 are allowed.

2. The following is an examiner's statement of reasons for allowance: The prior art of record primarily teaches two different structures for CMOS devices having a PMOS transistor with a SiGe channel and an NMOS transistor having a strained Si channel. In the first case, a thermal silicon oxide gate oxide layer is grown on both the SiGe in the PMOS channel region and the strained Si in the NMOS channel region (see U.S. Patent No. 5,847,419 to Imai et al.), and in the second case, a high dielectric constant metal oxide layer is deposited as the gate oxide for both the NMOS and PMOS (see U.S. Patent No. 6,310,367 to Yagishita). Although a person skilled in the art would recognize that either a high dielectric constant metal oxide or a relatively lower dielectric constant silicon oxide could be used as the gate oxide layer for either the NMOS or the PMOS, there is no real motivation in the prior art to combine these structures and specifically select a high dielectric constant metal oxide as the PMOS gate oxide and a silicon oxide film as the NMOS gate oxide.

Considering the additional fabrication steps and difficulty that would be required to form different gate oxides for each of the NMOS and PMOS devices, it is the examiner's opinion that a person skilled in the art would not have considered it advantageous or obvious in any way to use different materials for the gate oxide layers in order to meet the limitations of the claims. Furthermore, since the specific combination of channel and gate dielectric materials for the NMOS and PMOS devices also provides the unexpected result of providing substantially equal

drive currents for the NMOS and PMOS devices (see specification, pages 4-5), it is the Examiner's opinion that selection of the specifically claimed combination of materials based on the broad 'equivalence' and 'known use' teachings of the prior art would purely be based upon impermissible hindsight.

It is additionally noted that although the prior art does suggest instances in which it might be advantageous to use different gate oxides for a CMOS device (as in U.S. Patent No. 5,970,331 to Gardner et al.), these instances require a metal gate in the PMOS and a polysilicon gate in the NMOS. Since the closest prior art, as discussed above, uses the exact same gate materials for both the NMOS and PMOS devices, and since there is no particular motivation provided in any of the references for using different gate materials for each type of MOS, the Examiner does not consider these teachings to be reasonably combinable with the other prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd